WHAT IS CLAIMED IS:

1. A method for clamping a semiconductor wafer having a backside insulator to a J-R electrostatic chuck having a leaky dielectric layer, the method comprising:

determining a single-phase square wave clamping voltage for the electrostatic chuck, wherein the determination is based, at least in part, on a minimum residual clamping force associated with the wafer and the electrostatic chuck and a surface topography of the leaky dielectric layer;

placing the wafer on the electrostatic chuck; and

applying the determined single-phase square wave clamping voltage to the electrostatic chuck, therein electrostatically clamping the wafer to the electrostatic chuck, wherein at least the minimum residual clamping force is maintained during a polarity switch of the single-phase square wave clamping voltage, wherein the wafer remains clamped to the electrostatic chuck.

2. The method of claim 1, wherein the surface topography of the leaky dielectric layer comprises a first gap and a second gap between the wafer and the electrostatic chuck, wherein an *RC* time constant is associated with the respective first gap and second gap, and wherein a difference between the *RC* time constant associated with the respective first gap and second gap is such that at least the minimum residual clamping force is maintained during the polarity switch of the determined single-phase square wave clamping voltage.

3. The method of claim 2, wherein the second gap is associated with a natural surface roughness of the leaky dielectric layer, and wherein the first gap is larger than the second gap.

4. The method of claim 3, wherein the first gap is at least twice as large as the second gap.

5. The method of claim 3, wherein the first gap is at least three times as large as the second gap.

6. The method of claim 5, wherein the first gap is approximately 4 microns, and wherein the second gap is approximately 1 micron.

7. The method of claim 3, wherein the first gap is formed into the leaky dielectric layer by conventional machining or micro-machining the leaky dielectric layer.

8. The method of claim 2, wherein determining the single-phase square wave clamping voltage comprises determining a waveform defined by a pulse width and a pulse magnitude, wherein the waveform is a function the *RC* time constant associated with the respective first gap and second gap.

9. The method of claim 8, wherein the pulse magnitude is determined such that at least the minimum residual clamping force is provided between the wafer and the electrostatic chuck.

10. The method of claim 8, wherein the pulse magnitude of the determined single-phase square-wave clamping voltage is approximately less than +/- 300 volts.

11. The method of claim 8, further comprising stopping the determined single-phase square wave clamping voltage, therein de-clamping the wafer from the electrostatic chuck, wherein a de-clamping time is associated with the pulse width of the determined waveform.

12. The method of claim 11, wherein the pulse width of the determined waveform is shorter than a required de-clamping time which satisfies process throughput specifications.

13. The method of claim 11, wherein the pulse of the determined waveform is less than approximately 1 second.

14. The method of claim 1, further comprising determining the surface topography of the leaky dielectric layer.

15. The method of claim 14, wherein determining the surface topography comprises determining one or more of an island height and an island area ratio.

16. The method of claim 1, further comprising applying a cooling gas backpressure to a backside of the wafer through the electrostatic chuck, wherein the determined single-phase square wave clamping voltage is further determined based on the cooling gas backpressure.

17. A system for clamping a wafer having a backside insulator, the system comprising:

a J-R electrostatic chuck comprising a leaky dielectric layer and one or

more electrodes operable to provide an electrostatic clamping force between the leaky dielectric layer and the wafer, the leaky dielectric layer having a plurality of islands extending from a surface thereof, whereon the wafer resides, wherein a first gap is defined between the surface of the dielectric layer and the wafer, and a second gap is defined between a top surface of the plurality of islands and the wafer, wherein the first gap and the second gap, in conjunction with the leaky dielectric layer, further define a respective *RC* time constant associated therewith; and

a power supply configured to provide a single-phase square wave clamping voltage to the one or more electrodes, wherein a pulse magnitude of the single-phase square wave clamping voltage is associated with the *RC* time constant of the respective first gap and the second gap, and wherein the J-R electrostatic chuck is operable to maintain a minimum residual clamping force during a polarity switch of the single-phase square wave clamping voltage due, at least in part, to the respective *RC* time constants.

18. The system of claim 17, wherein the second gap is defined by a natural surface roughness of the leaky dielectric layer.

19. The system of claim 18, wherein the natural surface roughness of the leaky dielectric layer is approximately 1 micron or less.

20. The system of claim 17, wherein the first gap is at least twice as large as the second gap.

21. The system of claim 17, wherein the first gap is at least three times as large as the second gap.

22. The system of claim 17, wherein the first gap is approximately 4 microns, and wherein the second gap is approximately 1 micron.

23. The system of claim 17, wherein the plurality of islands are formed by one or more of conventionally machining and micro-machining the leaky dielectric layer, wherein a portion of the leaky dielectric layer is removed, therein defining the first gap between the wafer and the surface of the leaky dielectric layer.

24. The system of claim 23, wherein the plurality of islands are formed by bead blasting the leaky dielectric layer.

25. The system of claim 17, wherein a pulse magnitude of the single-phase square wave clamping voltage is operable to provide at least the minimum residual clamping force to the wafer.

26. The system of claim 17, wherein a pulse width of the single-phase square wave clamping voltage is shorter than a required de-clamping time which satisfies process throughput specifications.

27. The system of claim 17, further comprising a cooling gas supply, wherein the cooling gas supply is operable to provide a cooling gas backpressure between the electrostatic chuck and the wafer, and wherein the cooling gas backpressure is further associated with the minimum residual clamping force.